In the Claims

Claim 5 is amended.

Claims 5-24 remain in the application and are listed as follows:

1.-4. (Canceled).

5. (Currently Amended) ~~The method of claim 1~~ A method of processing data using a transmit parallel interface comprising:

providing a system clock signal associated with data in a first clock domain;

providing a high speed clock signal relative to the system clock signal;

dividing the high speed clock signal to provide a clock signal in a second clock domain; and

clocking data using the clock signal in the second clock domain, wherein the system clock signal has rising and falling clock edges, and said dividing the high speed clock signal to provide the clock signal in the second clock domain comprises doing so in a manner that places a rising edge of the clock signal in the second clock domain around the falling edge of the system clock signal.

6. (Original) A method of processing data using a transmit parallel interface comprising:

clocking input data, in a parallel state, using a first clock signal to produce clocked input data, the first clock signal having a frequency;

clocking a reset signal using the system clock signal to produce a clocked reset signal;

clocking the clocked reset signal using a high speed clock signal to produce an output signal;

receiving both the high speed clock signal and the output signal with a divider circuit;

using the output signal to reset the divider circuit effective to produce a second clock signal having a frequency that is the same as the frequency of the first clock signal; and

re-clocking the clocked input data using the second clock signal.

7. (Original) The method of claim 6, wherein said using of the output signal to reset the divider circuit produces a second clock signal having a rising edge close to a falling edge of the first clock signal.

8. (Original) The method of claim 6 further comprising after said re-clocking, serializing re-clocked input data for transmission in a serial state.

9. (Original) The method of claim 6, wherein the clocked reset signal and the clocked input data are matched.

10. (Original) The method of claim 6, wherein the first clock signal is of a dividable frequency of the high speed clock signal.

11. (Original) A transmit parallel interface comprising:

a single chip;

integrated circuitry on the chip configured to:

clock input data, in a parallel state, using a first clock signal to produce clocked input data, the first clock signal having a frequency;

clock a reset signal using the system clock signal to produce a clocked reset signal;

clock the clocked reset signal using a high speed clock signal to produce an output signal;

receive both the high speed clock signal and the output signal with a divider circuit;

produce, with the divider circuit, a second clock signal that has a frequency that is the same as the frequency of the first clock signal; and

re-clock the clocked input data using the second clock signal.

12. (Original) A transmit parallel interface comprising:

a first circuit to receive a clocked reset signal and a high speed clock signal and produce therefrom an output signal, the clocked reset signal being clocked by a system clock signal associated with a first clock domain and having a first frequency; and

a second circuit to receive the high speed clock signal and the output signal from the first circuit to produce therefrom a clock signal in a second clock domain, said second clock domain clock signal having a second frequency that is the same as the first frequency of the system clock signal.

13. (Original) The transmit parallel interface of claim 12, wherein the second circuit comprises a divider circuit.

14. (Original) The transmit parallel interface of claim 12, wherein the second circuit produces its clock signal such that a rising edge of the produced clock signal is located close to a falling edge of the system clock signal.

15. (Original) The transmit parallel interface of claim 12, wherein the system clock signal is at a dividable frequency of the high speed clock signal.

16. (Original) The transmit parallel interface of claim 12, wherein the high speed clock signal is greater than or equal to 4 times faster than the system clock signal.

17. (Original) The transmit parallel interface of claim 12, wherein the first circuit comprises one or more flip flops that are clocked by the high speed clock signal.

18. (Original) The transmit parallel interface of claim 12, wherein the first and second circuits are disposed on a single chip.

19. (Original) A transmit parallel interface comprising:

a first assembly of one or more flip flops configured to receive input data in a parallel state and clock the input data using a system clock signal to produce clocked input data, the system clock having a frequency;

a second assembly of one or more flip flops configured to receive a reset signal and clock the reset signal with the system clock signal to produce a clocked reset signal;

a third assembly of one or more flip flops configured to receive the clocked reset signal and clock the clocked reset signal with a high speed clock signal to produce an output signal;

a circuit configured to receive the output signal and the high speed clock signal and produce therefrom a clock signal that has the same frequency as the system clock signal;

a fourth assembly of one or more flip flops configured to receive the clocked input data and re-clock the clocked input data using the clock signal having the same frequency as the system clock; and

a serializer to serialize the re-clocked clocked input data.

20. (Original) The transmit parallel interface of claim 19, wherein the system clock signal is a dividable frequency of the high speed clock signal.

21. (Original) The transmit parallel interface of claim 19, wherein the first, second, third and fourth assemblies of flip flops, as well as said circuit and serializer are disposed on a single integrated circuit chip.

22. (Original) The transmit parallel interface of claim 19, wherein said circuit comprises a divider circuit.

23. (Original) The transmit parallel interface of claim 19, wherein said circuit comprises a 1/N divider circuit, where N is greater than or equal to 4.

24. (Original) The transmit parallel interface of claim 19, wherein said clock signal having the same frequency as the system clock is produced to have a rising edge located very close a falling edge of the system clock signal.